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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MASON, DONNA K	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/736,927	BAR-OR, SHAHAR	
	Examiner	Art Unit	
	Donna K. Mason	2111	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-18* is/are rejected.

7)☒ Claim(s) *17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 17 is objected to because of the following informalities: In line 8, change "UARTs" to --UART--. Appropriate correction is required. See 37 CFR 1.75.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4 and 6-18 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,884,102 to England, et al. ("England").

With regard to claim 1, England discloses a method for controlling data communications between an external interface and at least first and second chips, the first chip having a first universal asynchronous receiver-transmitters (UART), a first microcontroller, and a switching mechanism capable of connecting the first UART and the first microcontroller, and the second chip having a second microcontroller and a second UART connecting the second microcontroller to the first UART, the method including: monitoring signals communicated to the first chip (Fig. 3A, item 310) from at least one of the external interface (Fig. 3A, item 308) and the second UART (Fig. 3A, item 316); and communicating data between the external interface (Fig. 3A, item 308) and the second microcontroller (Fig. 3A, item 312) via the first and second UARTs, in

response to the switching mechanism detecting a predetermined signal (Fig. 3A, item 318; and *see generally*, column 3, lines 11-67 to column 4, lines 1-67), as recited in claim 1.

With regard to claims 2-4, England discloses the method, where the predetermined signal is a switch sequence received from at least one of the second UART and the external interface; communicating data between the external interface and the first microcontroller, after the switching mechanism has detected that a time-out period has expired; and where the switching mechanism is implemented as control software executing over the first microcontroller (*see generally*, column 3, lines 20-22; and Fig. 3A, item 318; and *see generally*, column 3, lines 11-67 to column 4, lines 1-67), as recited in claims 2-5.

With regard to claims 6 and 11, England discloses a computing system, and method thereof, the computing system including a first chip (Fig.3A, item 310). The first chip includes a first UART (Fig. 3A, item 317), a second UART (Fig. 3A, item 316), a switch mechanism (Fig. 3A, item 318 and Fig. 3B, item 318) and a first microcontroller (Fig. 3A, item 312), where the first UART is in communication with an external interface (Fig. 3A, item 311) and the first UART is connectable to the second UART and the first microcontroller via the switch mechanism. The computing system also includes a second chip (Fig. 3A, item 300) including a second microcontroller (Fig. 3A, item 300) and a third UART (Fig. 3A, item 309) connected between the second UART and the second microcontroller; where the switch mechanism causes data to be routed between the second microcontroller and the external interface via the first, second and third

UARTs, in response to detecting a first logic level (*see generally*, column 3, lines 11-67 to column 4, lines 1-67), as recited in claim 6, and as similarly recited in claim 11.

With regard to claims 7-10 and 12-16, England discloses where the switch mechanism causes data to be routed between the external interface and the first microcontroller via the first UART, in response to detecting a second logic level (column 3, lines 45-67 to column 4, lines 1-22); where the switch mechanism is implemented in either software or hardware, or both software and hardware (column 3, lines 20-22); and where the first and second logic levels have equal values (column 3, lines 45-67 to column 4, lines 1-22), as recited in claims 12-16 and as similarly recited in claims 7-10.

With regard to claim 17, England discloses a method for controlling data communications between an external interface (Fig. 3A, item 306) and first and second chips (Fig. 3A, items 310 and 300), the first chip including first and second universal asynchronous receiver-transmitters (UARTs) (Fig. 3A, items 317 and 316) and the second chip having a third UART (Fig. 3A, item 309) the method including: monitoring signals communicated from the external interface to the first UART: and routing data from the first UART to the third UART, via the second UART, in response to detecting a switch signal (Fig. 3A, item 318; and *see generally*, column 3, lines 11-67 to column 4, lines 1-67), as recited in claim 17.

With regard to claim 18, England discloses the method, further including: monitoring signals communicated from the third UART to the second UART; and routing data from the third UART to the first UART, via the second UART, in response to

detecting a switch signal (Fig. 3A, item 318; and *see generally*, column 3, lines 11-67 to column 4, lines 1-67).

Therefore, England discloses the invention as specified in claims 1-4 and 6-18.

4. Claim 5 is rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,214,584 to Dingee, et al. ("Dingee").

With regard to claim 5, Dingee discloses a method for controlling data communications between an external interface connected in series to a plurality of chips, the method including: monitoring signals communicated to a first chip (Fig. 2, item 24) from at least one of the external interface and a second chip (Fig. 2, item 10) from the plurality of chips, where the first chip is connected between the external interface (*see* Fig. 2, which shows an interface formed between items 24 and 76) and the second chip (Fig. 2, item 10); and communicating data between the external interface and the second chip via the first chip, in response to a switching mechanism (Fig. 2, item 40) in the first chip detecting a predetermined signal (Fig. 2, items 28a and 28b). Also, *see generally*, column 6, lines 27-63).

Therefore, Dingee discloses the invention as specified in claim 5.

Conclusion

5. A shortened statutory period for reply is set to expire THREE MONTHS from the mailing date of this communication. Extensions of time may be available under the

provisions of 37 CFR 1.136(a). In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this communication.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna K. Mason whose telephone number is (571) 272-3629. The examiner can normally be reached on Monday - Friday, 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DKM

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